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Attorney's Docket No. 67,200-367 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chang et al
Serial No.: 09/ 821,554
Filed: March 29, 2001
For: Dual Damascene Method Employing Composite Low Dielectric Constant Dielectric Layer Having Intrinsic Etch Stop Characteristics

Group Art Unit: 1765
Examiner: Lynette T. Umez Eronini

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on July 22, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

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A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$160.00
X	other than a small entity	$320.00

Appeal Brief fee due: $ 320.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 282 673 426 US in an envelope addressed to Mail Stop: Appeal, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

Dated: 9-22-03

Kathy Dixon

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4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 390.00	$195.00
☐	three months	$ 930.00	$465.00
☐	four months	$1,470.00	$735.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 320.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 320.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 320.00
X Charge Visa Credit Card No. 4756 8461 9568 0263 the sum of $ 320.00.
A duplicate copy of this transmittal is attached.

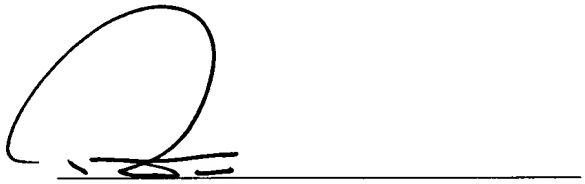
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge Visa Credit Card No. 4756 8461 9568 0263

And/Or

__X__ If any additional fee for claims is required, please charge Visa Credit Card No. 4756 8461 9568 0263



Signature of Attorney

Registration No. 31,311

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67,200-367; TSMC 00-407
Serial Number 09/821,554

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PATENT & TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF

TO: Commissioner for Patents
Washington, D.C. 20231

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 18 August 2003

REF:

Applicant	:	Chang et al.	Filing Date	:	29 March 2001
Serial No.	:	09/821,554	Att'y No.	:	67,200-367; TSMC 00-407
Art Unit	:	1765	Examiner	:	Lynette T. Umez Eronini
Title	:	Dual Damascene Method Employing Composite Low Dielectric Constant Dielectric Layer Having Intrinsic Etch Stop Charaacteristics			

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 282 673 426 US
Date of Deposit Sept. 22, 2003

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $320.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 22 April 2003 and made FINAL, applicant filed a notice of appeal on 22 July 2003. In accord with applicant's notice of appeal, please accept this appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-15 are pending in this application. Claims 1, 3-4, 7-8, 10-11 and 14-15 are finally rejected under 35 U.S.C. § 102(e). Claims 2, 5-6, 9 and 12-13 are finally rejected under 35 U.S.C. § 103(a). Appeal is taken for claims 1-15 as finally rejected under 35 U.S.C. § 102(e) or 103(a).

4. Status of the Amendments

A response, filed 18 June 2003, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 23 June 2003, the Examiner indicated that applicant's response was considered but did not place applicant's application in condition for allowance. The Examiner also indicated that applicant's response would be entered.

5. Summary of the Invention

The invention provides a dual damascene method for forming within a microelectronic fabrication a contiguous patterned conductor interconnect and patterned conductor stud layer within a corresponding trench contiguous with a corresponding via formed in turn formed through a dielectric layer formed of a comparatively low dielectric constant dielectric material, with enhanced microelectronic fabrication processing efficiency. (page 10, first full paragraph)

The invention realizes the foregoing object by employing when forming an aperture through a dielectric layer in accord with a dual damascene method and further in accord with the present invention, a composite dielectric layer comprising: (1) a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via; and (2) a blanket second dielectric layer formed upon the patterned first dielectric layer and filling the via, the blanket second dielectric layer being formed of a second dielectric material having a second dielectric constant of less than about 4.0; where (3) the patterned first dielectric layer serves as an intrinsic etch stop within an anisotropic etch method employed for etching the blanket second dielectric layer to form therethrough an aperture comprising: (1) a trench; contiguous with (2) at least a portion of the via. (paragraph bridging pages 10-11)

The invention is claimed in two levels of scope including: (1) a method for forming an aperture through a dielectric layer (independent claims 1 and 4 and dependent claims 2-3 and 5-7); and (2) a derivative method for forming a patterned conductor layer within the aperture through the dielectric layer (independent claims 8 and 11 and dependent claims 9-10 and 12-15).

Independent claim 1 is read on the specification and drawings as follows:

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate 10 (Fig. 1; and page 14, second full paragraph);

forming upon the substrate 10 a patterned first dielectric layer 14a/14b/14c formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer 14a/14b/14c defining a via 15a/15b (Fig. 1; and page 17, first paragraph to page 19, first paragraph);

forming upon the patterned first dielectric layer 14a/14b/14c and filling the via 15a/15b a blanket second dielectric layer 16 formed of a second dielectric material having a second dielectric constant of less than about 4.0 (Fig. 1; and page 19, second paragraph to page 20, first full paragraph);

forming over the blanket second dielectric layer a patterned mask layer 18a/18b/18c which defines the location of a trench 19 to be formed through the blanket second dielectric layer 16, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via 15a/15b (Fig. 1; and page 20, second full paragraph to page 21, first full paragraph); and

etching, while employing the patterned mask layer 18a/18b/18c in conjunction with an anisotropic etch method, the blanket second dielectric layer 16 to form an aperture 23a/23b comprising:

the trench 21a/21b; and

at least a portion of the via 15a/15b, where the patterned first dielectric layer 14a/14b/14c provides an intrinsic etch stop within the anisotropic etch method (Fig. 2; and page 22, first full paragraph to page 23, first full paragraph).

6. Issues

I. Whether claims 1, 3-4, 7-8, 10-11 and 14-15 may properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Somekh (U.S. Patent No. 6,292,334).

II. Whether claims 2, 5-6, 9 and 12-13 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Yu et al. (U.S. Patent No. 6,004,883; hereinafter "Yu").

7. Grouping of Claims

Claims 1-7, group I, are directed towards a first claimed embodiment of the invention.

Claims 8-15, group II, are directed towards a second claimed embodiment of the invention.

The claims do not stand or fall together within their respective groups.

8. Argument

I. The claims do not stand or fall together within their respective groups.

Applicant notes that applicant's amended claim 4 and amended claim 11 have contained therein a specific limitation of absence of a hard mask layer interposed between applicant's patterned first dielectric layer and applicant's blanket second dielectric layer. Since the explicit absence of a patterned hard mask layer is an issue within prosecution of applicant's

claims to applicant's invention, applicant specifically requests independent consideration of each of applicant's independent claims 1, 4, 7 and 11.

II. Claims 1, 3-4, 7-8, 10-11 and 14-15 may not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Somekh.

III. Claims 2, 5-6. 9 and 12-13 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Yu.

a. Somekh Subject Matter

Somekh (abstract and Fig. 4a to Fig. 4h) discloses a method for forming a dual damascene structure which employs a patterned amorphous carbon etch stop layer interposed between a blanket first dielectric layer and a blanket second dielectric layer..

b. Yu Subject Matter

Yu (abstract and cover figure) discloses a dual damascene patterned conductor layer formation method without an etch stop layer. The method employs a patterned first dielectric layer formed of a first dielectric material which is not susceptible to etching within an oxygen containing plasma, in conjunction with a blanket second dielectric layer formed of a second dielectric material which is susceptible to etching within the oxygen containing plasma.

c. The Examiner's Assertions

Within: (1) the paragraph bridging pages 2-3; (2) page 6, fourth paragraph; (3) page 9, last clause; and (4) page 13, third paragraph, of the office action made FINAL, the Examiner asserts that Somekh's low k etch stop layer 14 corresponds with applicant's patterned first dielectric layer within applicant's dual damascene structure.

Within: (1) page 5, last paragraph; (2) page 9, first paragraph; (3) page 12, fourth paragraph); and (4) page 16, third paragraph, of the office action made FINAL, the Examiner does not apparently provide a proper basis for suggestion or motivation for modification or combination of Somekh and Yu to provide for rejection of applicant's claims to applicant's invention under 35 U.S.C. § 103. MPEP 2142, 2143, 2143.01.

d. Applicant's Response

In response in a first instance, applicant respectfully disagrees in part with the Examiner's reading of Somekh insofar as the Examiner asserts within: (1) the paragraph bridging pages 2-3; (2) page 6, fourth paragraph; (3) page 9, last clause; and (4) page 13, third paragraph, of the office action made FINAL that Somekh's low k etch stop layer 14 corresponds with applicant's patterned first dielectric layer within applicant's dual damascene structure. Rather, Somekh at col. 3, last full paragraph clearly designates Somekh's reference numeral 10 as Somekh's first dielectric layer within Somekh's dual damascene structure. Somekh's first dielectric layer is a blanket first dielectric layer within a damascene structure, rather than a patterned first dielectric layer within a damascene structure, as disclosed and claimed by applicant within claim 1, amended claim 4, claim 8 and amended claim 11 (clauses 2).

In addition, applicant notes that since Somekh's blanket first dielectric layer 10 and blanket second dielectric layer 18 are formed of a fluorosilicate glass (FSG) dielectric material (col. 4, lines 20-25 and 60-65) Somekh's blanket first dielectric layer 10 will inherently not provide an intrinsic etch stop with respect to Somekh's blanket second dielectric layer 18, as required within applicant's invention as disclosed and claimed within claim 1, amended claim 4, claim 8 and amended claim 11 (clauses 7).

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1, amended claim 4, claim 8 and amended claim 11 is not disclosed within Somekh, in particular with respect to a first dielectric layer within a dual damascene method being formed as a patterned first dielectric layer which provides an intrinsic etch stop when etching a blanket second dielectric layer formed thereupon, applicant asserts that claim 1, amended claim 4, claim 8 and amended claim 11 may not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Somekh.

Since all remaining claims within the foregoing rejections are dependent upon claim 1 or claim 8 and carry all of the limitations of claim 1 or claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Somekh or under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Yu.

In response in a second instance, and in particular with respect to amended claim 4 and amended claim 11, applicant additionally asserts that those claims may also not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Somekh insofar as those claims specifically require absence of a hard mask layer interposed between applicant's patterned first dielectric layer and applicant's blanket second dielectric layer (clauses 3). In comparison, Somekh (abstract and Figs. 4a to 4f) inapposite thereto discloses a dual damascene method specifically including a patterned hard mask layer interposed between a blanket first dielectric layer and a blanket second dielectric layer.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of: (1) claims 1, 3-4, 7-8, 10-11 and 14-15 under 35 U.S.C. § 102(e) as being anticipated by Somekh; and (2) claims 2, 5-6, 8 and 12-13 under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Yu, be withdrawn.

9. Summary

Applicant's invention as disclosed and claimed within claim 1, amended claim 4, claim 8 and amended claim 11 is directed towards a dual damascene method for forming: (1) an aperture through a dielectric layer; and (2) a patterned conductor layer within the aperture. The dual damascene method employs a patterned first dielectric layer having formed thereupon a blanket second dielectric layer, absent an extrinsic etch stop layer formed interposed between the patterned first dielectric layer and the blanket second dielectric layer. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within claim 1, amended claim 4, claim 8 and amended claim 11.

10. Conclusion

Applicant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims remaining within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,

Randy W. Tung (Reg. No. 31,311)

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Bloomfield Hills, MI 48302
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248-540-4035 (facsimile)

APPENDIX

COMPLETE COPY OF THE CLAIMS

1. (original) A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

2. (original) The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. (original) The method of claim 1 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

4. (previously amended) A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0, where there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

5. (original) The method of claim 1 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

6. (original) The method of claim 1 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

7. (original) The method of claim 1 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

8. (original) A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

9. (original) The method of claim 8 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

10. (original) The method of claim 8 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

11. (previously amended) A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0, where there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

12. (original) The method of claim 8 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

13. (original) The method of claim 8 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

14. (original) The method of claim 8 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

15. (original) The method of claim 8 wherein the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method.